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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,156	08/09/2001	Joseph E. Algieri	10006369-1	3994

7590 03/09/2005
HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

GARCIA OTERO, EDUARDO

ART UNIT PAPER NUMBER

2123

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/927,156

Applicant(s)

ALGIERI ET AL.

Examiner

Eduardo Garcia-Otero

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION: Non-Final (first action on the merits)

Introduction

1. Title is: TECHNIQUE AND INTERFACE FOR STORAGE SYSTEM RESOURCE ASSIGNMENT.
2. First listed inventor is: ALGIERI.
3. Claims 1-31 are pending.
4. US Application received 8/12/2001, and no earlier priority is claimed.

Index of Important Prior Art

5. Smith refers to "HDL Chip Design" by Douglas J. Smith, 1996, Ninth printing 2001 minor updates, ISBN 0-9651934-3-8, pages 2-19.
6. Tufte refers to The Visual Display of Quantitative Information, Edward Tufte, Graphics Press, 1983, page 126.
7. Juran refers to Juran on Quality by Design, by J. M. Juran, The Free Press, 1992, ISBN 0-02-916683-7, page 462-467 on Taurus.
8. Mason refers to US Patent 6,487,562.
9. Markosian refers to US Patent 6,446,239.
10. Greidinger refers to US Patent 6,449,761.

Definitions

11. **Field Programmable Gate Array (FPGA)** is defined as "A device containing many circuits whose interconnections and functions are programmable by the user. Note: Generally larger than a field programmable logic array. See also: dynamically programmable logic gate", according to The Authoritative Dictionary of IEEE Standards and Terms, Seventh Edition, by IEEE Press, ISBN 0-7381-2601-2, 2000.

35 USC § 112-Second Paragraph-indefinite claims

12. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
13. Claims 1 and 2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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14. In claims 1 and 2, claim 1 states “the storage system”, and claim 2 states “a data storage system”. It is not clear whether both claims are referring to the same type of storage. It is not clear what is the antecedent basis for “the storage system” in claim 1. It is not clear how claim 2 further limits claim 1, as required by 35 USC 112 paragraph 4 “claim in dependent form... specify a further limitation”.
15. In claim 4, the term “utility functions” is not adequately defined.
16. In claims 8 and 9, the terms “first indicia” and “second indicia” are not adequately defined.

Specification

17. At specification page 10 line 4, please insert the missing US Patent serial number into the blank space, which appears to be 09/924,735.

Knowledge based expert systems

18. As a preface to the 35 USC 112 rejections, it appears useful to review three examples of knowledge based expert systems, as well as the relevant cases and burdens.
19. DEFINITION. The claimed invention appears to be a relatively low-level expert system. An “expert system” is defined by Microsoft Computer Dictionary as “An application program that makes decisions or solves problems in a particular field, such as finance or medicine, by using knowledge and analytical rules defined by experts in the field. It uses two components, a knowledge base and an inference engine, to form conclusions... See also artificial intelligence, inference engine, intelligent database, knowledge base.”
20. THREE EXAMPLES. The complexity of early expert systems is discussed by Time-Life Artificial Intelligence (copyright 1986) at page 40 “With considerable help and encouragement from Feigenbaum and his colleague Bruce Buchanan, another Stanford research scientist, Shortliffe devised an expert system dubbed MYCIN. Armed with some 500 if-then rules for diagnosing meningitis and blood infections and recommending antibiotic therapies”.
21. A second expert system is discussed at page 41, “CADUCEUS-which was named for the traditional winged-staff-and-serpent symbol of physicians-began in the early 1970s. Its goal is to encompass the essential diagnostic knowledge of some 700

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diseases. With Jack Meyers serving as an important source of the system's expertise, it is perhaps unsurprising that CADUCEUS acquired the nickname Jack-in-the-Box.... Systems such as CADUCEUS are severely limited by the size of their knowledge bases."

22. A third expert system is discussed at page 41, "Aldo Cimino... expert in maintaining the complex sterilizers, or "cookers," used for killing bacteria in canned soup... spent about seven months with Michael Smith, a so called knowledge engineer-a computer scientist who tries to reduce complex subjects to the if-then formant that can be processed by an expert system ... more than 150 rules of thumb to aid the operators of Cambell's sterilizers". Note that two experts spent seven months (or 14 man-months, or more than 1 man-year) to generate 150 if-then rules.
23. LEGAL PRECEDENT. For the record, note two useful cases regarding enablement. *White Consolidated Industries, Inc. v. Vega Servo-Control Inc.* (CAFC) 218 USPQ 961, 963 (7/25/83) addresses software enablement and states "The amount of required experimentation, however, must be reasonable" and "in this case that development of a single pass language translator would require from 1-1/2 to 2 manyears of effort, a clearly unreasonable requirement".
24. Also note that *In re Wands* (CA FC) 8 USPQ2d 1400, 1404 (9/30/1998) provides an 8 factor test for determining undue experimentation: "Factors to be considered in determining whether a disclosure would require undue experimentation...includes (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims".
25. MPEP BURDENS. Examiner bears "the initial burden to establish a reasonable basis to question the enablement" according to MPEP 2164.04. The burden then shifts to the Applicant to "present persuasive arguments, supported by suitable proofs where necessary", see MPEP § 2164.05. The standard for the Applicant's arguments is "convincing to one skilled in the art", see MPEP § 2164.05.

35 USC § 112- first paragraph- enablement

26. The following is a quotation of the first paragraph of 35 U.S.C. 112: The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
27. Claims 1-31 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
28. Specifically, all of the claims appear to claim an expert system for circuit design. For example, claim 1 limitation (b) states “modifying the design in response to said desired levels”, and limitation (c) states “predicting levels of performance parameters for the modified design of the storage system”. These appear to be expert system type functions that might be performed by Bachelor of Science in Electrical Engineering, or similar. No set of expert rules is provided by which said modifications or predictions would be enabled. See above discussion of expert systems.
29. Additionally, regarding claim 1 limitation (b) “modifying the design in response to said desired levels”, note that Juran page 465 states “The needed investment was enormous... 400+ features. For many of the rest, there were conscious tradeoffs to avoid suboptimization.” Thus, Juran discloses optimizing design by using multiple criteria optimization of an objective function, where there are 400+ features. Applicant’s specification (such as FIG 4) does not begin to enable design and optimization of a complex circuit, such as an FPGA. Note that according to Artificial Intelligence page 41, even just cooking soup takes 150 rules, and over 1 man-year to generate the 150 rules.
30. Please contrast the Applicant’s sparse FIG 4 against the detailed figures of Greidinger’s patent (such as Greidinger FIG 14A for example).
31. Additionally, note Specification page 2 admits “specialized skills are required to design and configure a storage system”.

Claim Rejections - 35 USC § 102(b)

32. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
33. Claim 1-5, 10-16, 21-22, and 23-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith
34. Claim 1 is an independent “method” claim with 4 limitations.
35. In claim 1 limitation (a), **“receiving desired levels of a performance parameters for a computer system design from a user via a user interface to a computer system”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.
36. In claim 1 limitation (b), **“modifying the design in response to said desired levels”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”.
37. In claim 1 limitation (c), **“predicting levels of performance parameters for the modified design of the storage system”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”.
38. In claim 1 limitation (d), **“displaying for the user indicia of the predicted levels of performance parameters for the modified design”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that FIG 1.4 states “Results

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compare”, which means that the modified design results are compared to the desired results.

39. In claim 2, **“the computer system design comprises a design for a data storage system”** is disclosed by Smith page 3 “any electronic equipment containing Application-Specific Integrated Circuits (ASICs), or Field-Programmable Gate-Arrays (FPGAs)”. ASICs and FPGAs disclose both memories and registers, which are types of data storage.
40. In claim 3, **“said modifying includes reducing said desired levels of performance parameters”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips.
41. In claim 4, **“said reducing is based on utility functions”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips.
42. In claim 5 limitation (a), **“receiving the utility functions via the user interface to the computer system”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.
43. In claim 5 limitation (b), **“storing said utility functions in a memory device of the computer system”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for

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designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.

44. Claim 10 is an independent “method” claim with 5 limitations.

45. In claim 10 limitation (a), **“receiving desired levels of a performance parameters for a computer system design from a user via a user interface to a computer system”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.

46. In claim 10 limitation (b), **“developing the design”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.

47. In claim 10 limitation (c), **“predicting levels of performance parameters for the modified design of the storage system”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.

48. In claim 10 limitation (d), **“comparing the predicted levels of performance parameters to the desired levels of performance parameters”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC

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manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.

49. In claim 10 limitation (e), **“modifying the design when the predicted levels are lower than the desired levels, said modifying being performed by the computer system”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.
50. In claim 11, **“the computer system design comprises a design for a data storage system”** is disclosed by Smith page 3 “any electronic equipment containing Application-Specific Integrated Circuits (ASICs), or Field-Programmable Gate-Arrays (FPGAs)”. ASICs and FPGAs disclose both memories and registers, which are types of data storage.
51. In claim 12, **“said developing comprises assigning system resources to applications to be served by the design”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips.
52. In claim 13, **“said assigning being performed by a design tool operating on the computer system”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.

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53. In claim 14, **“said modifying includes reducing said desired levels of performance parameters”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips.
54. In claim 15, **“said reducing is based on utility functions”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips.
55. In claim 16, **“receiving the utility functions via the user interface to the computer system”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.
56. In claim 21, **“repeating said steps of predicting and comparing after said modifying”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL (hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.
57. In claim 22, **“when the predicted levels are lower than the desired levels after said modifying, then notifying the user”** is disclosed by Smith FIG 1.3 “Architectural Design” and “layout synthesis”, and FIG 1.4 “High level HDL specification” and “Vender audits and sign off design for ASIC manufacture”, and FIG 1.14 “VHDL/Verilog” and “optimize”. Note that VHDL and Verilog are HDL

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(hardware description languages) used for designing chips. Note that VHDL and Verilog are advanced design and simulation languages which are inherently performed on a computer system.

58. Claims 23-27 are “apparatus” claims with the same limitations as “method” claims 10-16 and 21-22 above, and are rejected for the same reasons.

Claim Rejections - 35 USC § 103

59. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
60. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: Determining the scope and contents of the prior art. Ascertaining the differences between the prior art and the claims at issue. Resolving the level of ordinary skill in the pertinent art. Considering objective evidence present in the application indicating obviousness or nonobviousness.
61. Claim 6-9, and 17-20, and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Greidinger US Patent 6,449,761.
62. Claims 6-9 depend from independent claim 1.
63. The additional limitations are not expressly disclosed by Smith.
64. In claim 6, **“the desired levels of performance parameters are specified by the user through a graphical user interface”** is disclosed by Greidinger column 18 lines 26-41 “multiple design solutions... microprocessor design... a cache... buffers”, and column 20 lines 17-42 “graphical user interfaces (GUIs)... displayed comparatively as bar graphs using one or more parameters”.
65. In claim 7, **“the desired levels of performance parameters are specified by the user through a graphical user interface by the user manipulating heights of bar graphs shown on a display of the computer system”** is disclosed by Greidinger column 18 lines 26-41 “multiple design solutions... microprocessor design... a

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cache... buffers”, and column 20 lines 17-42 “graphical user interfaces (GUIs)... displayed comparatively as bar graphs using one or more parameters”.

66. In claim 8, **“each bar graph includes first indicia of the corresponding level of the performance parameter”** is disclosed by Greidinger column 18 lines 26-41 “multiple design solutions... microprocessor design... a cache... buffers”, and column 20 lines 17-42 “graphical user interfaces (GUIs)... displayed comparatively as bar graphs using one or more parameters”.
67. In claim 9, **“each bar graph includes second indicia of the corresponding level of the performance parameter”** is disclosed by Greidinger column 18 lines 26-41 “multiple design solutions... microprocessor design... a cache... buffers”, and column 20 lines 17-42 “graphical user interfaces (GUIs)... displayed comparatively as bar graphs using one or more parameters”.
68. MOTIVATION FOR CLAIMS 6-9. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Greidinger to modify Smith. One of ordinary skill in the art would have been motivated to improve Smith’s circuit design methods by graphically (bar graphs) displaying and contrasting performance parameters using bar charts so that the user can visually and quickly determine (pre-attentively process) the simulation results.
69. Claims 17-20 depend from independent claim 10.
70. The additional limitations are not expressly disclosed by Smith.
71. In claim 17, **“the user interface is a graphical user interface”** is disclosed by Greidinger column 18 lines 26-41 “multiple design solutions... microprocessor design... a cache... buffers”, and column 20 lines 17-42 “graphical user interfaces (GUIs)... displayed comparatively as bar graphs using one or more parameters”.
72. In claim 18, **“the desired levels of performance parameters are specified by the user through a graphical user interface by the user manipulating heights of bar graphs shown on a display of the computer system”** is disclosed by Greidinger column 18 lines 26-41 “multiple design solutions... microprocessor design... a cache... buffers”, and column 20 lines 17-42 “graphical user interfaces (GUIs)... displayed comparatively as bar graphs using one or more parameters”.

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73. In claim 19, **“each bar graph includes first indicia of the corresponding level of the performance parameter”** is disclosed by Greidinger column 18 lines 26-41 “multiple design solutions... microprocessor design... a cache... buffers”, and column 20 lines 17-42 “graphical user interfaces (GUIs)... displayed comparatively as bar graphs using one or more parameters”.
74. In claim 20, **“each bar graph includes second indicia of the corresponding level of the performance parameter”** is disclosed by Greidinger column 18 lines 26-41 “multiple design solutions... microprocessor design... a cache... buffers”, and column 20 lines 17-42 “graphical user interfaces (GUIs)... displayed comparatively as bar graphs using one or more parameters”.
75. MOTIVATION FOR CLAIMS 17-20. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Greidinger to modify Smith. One of ordinary skill in the art would have been motivated to improve Smith’s circuit design methods by graphically (bar graphs) displaying and contrasting performance parameters using bar charts so that the user can visually and quickly determine (pre-attentively process) the simulation results.
76. Claims 28-31 are “apparatus” claims with the same limitations as “method” claims 17-20 above, and thus are rejected for the same reasons.

Additional Cited Prior Art

77. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action.
78. Tufte is cited to provide historical background for the use of bar charts dating back to at least 1786. Specifically, *The Visual Display of Quantitative Information*, Edward Tufte, Graphics Press, 1983, bottom of page 126, discloses an early bar graph by Playfair titled “Exports and Imports of SCOTLAND” dated “June 7, 1786”. Note how the bottom two bars graphically display and contrast the exports and imports of Scotland to and from Ireland.
79. Mason US Patent 6,487,562 at Abstract discloses “A user interface (UI) allows a user or system administrator to easily observe and configure system parameters, preferably

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using a graphic user interface which allows a user to select system changes along a scale from minimum to maximum” and column 2 line 51 “make changes dynamically to the data storage system... thereby optimize the system” and column 3 line 1 “bar graphs and scales”.

Conclusion

80. All pending claims stand rejected.

Communication

81. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 571-272-3711. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner’s supervisor, Kevin Teska, can be reached at 571-272-3761. The fax phone number for this group is 703-872-9306.

* * * *



**SAMUEL BRODA, ESQ.
PRIMARY EXAMINER**